Amendments to the Specification

Please **replace** the paragraph beginning at page 1, line 21 with the following **amended** paragraph:

Increasing the sampling frequency will reduce the period of uncertainty and thus yield improved jitter performance. However, increasing the sampling frequency will yield more samples. In some electronic systems, bandwidth constraints limit the number of samples capable of being transmitted within a given interval. In such systems, limited opportunities exist for jitter performance improvement.

Please **replace** the paragraph beginning at page 1, line 26 with the following **amended** paragraph:

Thus, there is need for a technique that achieves increased jitter performance in bandwidth-limited systems.

Please **replace** the paragraph beginning at page 2, line 20 with the following **amended** paragraph:

FIGURE 1 depicts a prior art apparatus 10 for sampling an asynchronous digital signal 11 generated by a transmitter 12. The transmitter 12 can take the form of any type of digital device that produces an asynchronous digital output signal. In other words, the output signal 11 of the transmitter 12 changes states between a logic "1" level and a logic "0" level a periodically. The sampling apparatus 10 includes a receiver 14 coupled to the output of the transmitter 12 for detecting the state of the signal 11 in response to each of a sequence of periodic clock pulses 15 from a sample clock 16. The sample clock 16 generates m uniformly spaced clock pulses 15 during an interval of duration t. In the illustrated embodiment, m=5 although the value of m could be larger or smaller.

Please **replace** the paragraph beginning at page 3, line 33 and continuing onto page 4, lines 1-7 with the following **amended** paragraph:

FIGURE 4 depicts a timing chart that shows the relationship over time between the signal 11 generated by the transmitter 12 of FIG 2 and the pulses 150 generated by the clock 160. As shown in FIG. 4, during each sample interval of duration t, the receiver 140 of FIG. 1 3 receives a successive one of fifteen clock pulses 150. each pulse causing the receiver to sample the input signal 11. At the end of every interval t, the receiver 140 generates a five-bit word 200 whose first bit (hereinafter referred to as a "reference data" bit) indicates the state of the input signal 11. The remaining four bits collectively identity ~~of~~ the particular one of the fifteen clock cycles within the interval t during which the signal 11 changed state, assuming such a change occurred.